Listing of Claims:

1. (Currently Amended) A radiation-emitting thin-film semiconductor chip comprising:

an epitaxial multilayer structure comprising:

an active, radiation-generating layer,

a first main face, and

a second main face remote from the first main face for coupling out radiation generated in the active, radiation-generating layer, and

a reflective layer or interface,

wherein the first main face of the multilayer structure is coupled to the reflective layer or interface, and

wherein a patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by either one- or two-dimensional depressions forming convex elevations, each said convex elevation having an upper surface that is not contiguous with an upper surface of an adjacent elevation. ~~the convex elevations having a height (h1) at least as large as a distance (h2) between the patterned region and the active, radiation-generating layer.~~

2. (Previously Presented) The semiconductor chip as claimed in claim 1, further comprising a carrier element coupled to the first main face, wherein the reflective layer or interface is arranged between the carrier element and the multilayer structure.

3. (Cancelled).

4. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the elevations have a form of truncated pyramids or truncated cones or a trapezoidal cross-sectional form.

5. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the elevations have a form of cones or a triangular cross-sectional form.

6. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the elevations have a form of sphere segments or a circle segment cross-sectional form.

7. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the elevations have an inclination angle (β) of between approximately 30° and approximately 70°.

8. (Previously Presented) The semiconductor chip as claimed in claim 7, wherein the elevations have an inclination angle (β) of between approximately 40° and approximately 50°.

9. (Cancelled).

10. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the height (h1) of the elevations is approximately twice as large as the distance (h2) between the patterned region of the multilayer structure and the active, radiation-generating layer.

11. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein a cell size (d) of the elevations is at most approximately five times as large as the height (h1) of the elevations.

12. (Previously Presented) The semiconductor chip as claimed in claim 11, wherein the cell size (d) of the elevations is at most approximately three times as large as the height (h1) of the elevations.

13. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the reflective layer or interface coupled to the first main area of the multilayer structure has a reflectivity of at least 70%.

14. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the reflective layer or interface coupled to the first main area of the multilayer structure has a reflectivity of at least 85%.

15. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the multilayer structure is applied onto a carrier substrate either directly by the first main face or via the reflective layer.

16. (Previously Presented) The semiconductor chip as claimed in claim 15, wherein the reflective layer or the carrier substrate serves as a contact layer of the semiconductor chip.

17. (Previously Presented) The semiconductor chip as claimed in claim 1, further comprising a conductive, transparent layer applied onto the second main face of the multilayer structure.

18. (Previously Presented) The semiconductor chip as claimed in claim 1, further comprising a transparent protective layer applied onto the second main face of the multilayer structure.

19-43. (Cancelled).

44. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein each of the convex elevations is defined by two-dimensional depressions.

45. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure of the semiconductor chip is free of a growth substrate.

46. (Currently Amended) A radiation-emitting thin-film semiconductor chip comprising an epitaxial multilayer structure and a reflective layer or interface, the epitaxial multilayer structure comprising:

an active, radiation-generating layer,

a first main face, and

a second main face remote from the first main face for coupling out the radiation generated in the active, radiation-generating layer,

wherein the first main face of the multilayer structure is coupled to the reflective layer or interface, and

wherein a patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by either one- or two-dimensional depressions forming convex elevations, each said convex elevation having an upper surface that is not contiguous with an upper surface of an adjacent elevation. ~~the convex elevations having an inclination angle (ß) of between approximately 30° and approximately 70°.~~

47. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure of the semiconductor chip is free of a growth substrate.

48. (Previously Presented) The semiconductor chip as claimed in claim 46, further comprising a carrier element coupled to the first main face, wherein the reflective layer or interface is arranged between the carrier element and the multilayer structure.

49. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the elevations have a form of truncated pyramids or truncated cones or a trapezoidal cross-sectional form.

50. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the elevations have a form of cones or a triangular cross-sectional form.

51. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the elevations have an inclination angle (β) of between approximately 40° and approximately 50°.

52. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the elevations have a height (h1) at least as large as a distance (h2) between the patterned region and the active, radiation-generating layer.

53. (Previously Presented) The semiconductor chip as claimed in claim 52, wherein the height (h1) of the elevations is approximately twice as large as the distance (h2) between the patterned region and the active, radiation-generating layer.

54. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein a cell size (d) of the elevations is at most approximately five times as large as a height (h1) of the elevations.

55. (Previously Presented) The semiconductor chip as claimed in claim 54, wherein the cell size (d) of the elevations is at most approximately three times as large as the height (h1) of the elevations.

56. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the reflective layer or interface coupled to the first main area of the multilayer structure has a reflectivity of at least 85%.

57. (Previously Presented) The semiconductor chip as claimed in claim 47, wherein the multilayer structure is applied onto a carrier substrate either directly by the first main face or via the reflective layer or interface.

58. (Previously Presented) The semiconductor chip as claimed in claim 57, wherein the reflective layer or interface or the carrier substrate serves as a contact layer of the semiconductor chip.

59. (Previously Presented) The semiconductor chip as claimed in claim 46, further comprising a conductive, transparent layer applied onto the second main face of the multilayer structure.

60. (Previously Presented) The semiconductor chip as claimed in claim 46, further comprising a transparent protective layer applied onto the second main face of the multilayer structure.

61. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the multilayer structure comprises a material or a plurality of different materials based on GaN.

62. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the second main face is a noncontinuous layer.

63. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the reflective layer is in direct contact with the epitaxial multilayer structure.

64. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on a II-VI semiconductor material.

65. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on a phosphide compound semiconductor material.

66. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on an arsenide compound semiconductor material.

67. (Previously Presented) The semiconductor chip as claimed in claim 1, wherein the patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by two-dimensional depressions forming convex elevations.

68. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the second main face is a noncontinuous layer.

69. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the reflective layer is in direct contact with the epitaxial multilayer structure.

70. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on a II-VI semiconductor material.

71. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on a phosphide compound semiconductor material.

72. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on an arsenide compound semiconductor material.

73. (Previously Presented) The semiconductor chip as claimed in claim 46, wherein the patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by two-dimensional depressions forming convex elevations.

74. (New) The semiconductor chip as claimed in claim 1, wherein the convex elevations have a height (h1) at least as large as a distance (h2) between the patterned region and the active, radiation-generating layer.

75. (New) The semiconductor chip as claimed in claim 46, wherein the convex elevations have an inclination angle (ß) of between approximately 30° and approximately 70°.